

Blackfin CMOS Camera Add-On-Card

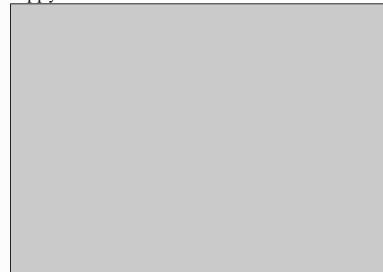
CAM Interface
CAM Interface.SchDoc



Platform Interface
Platform Interface.SchDoc



Supply Clock
Supply Clock.SchDoc

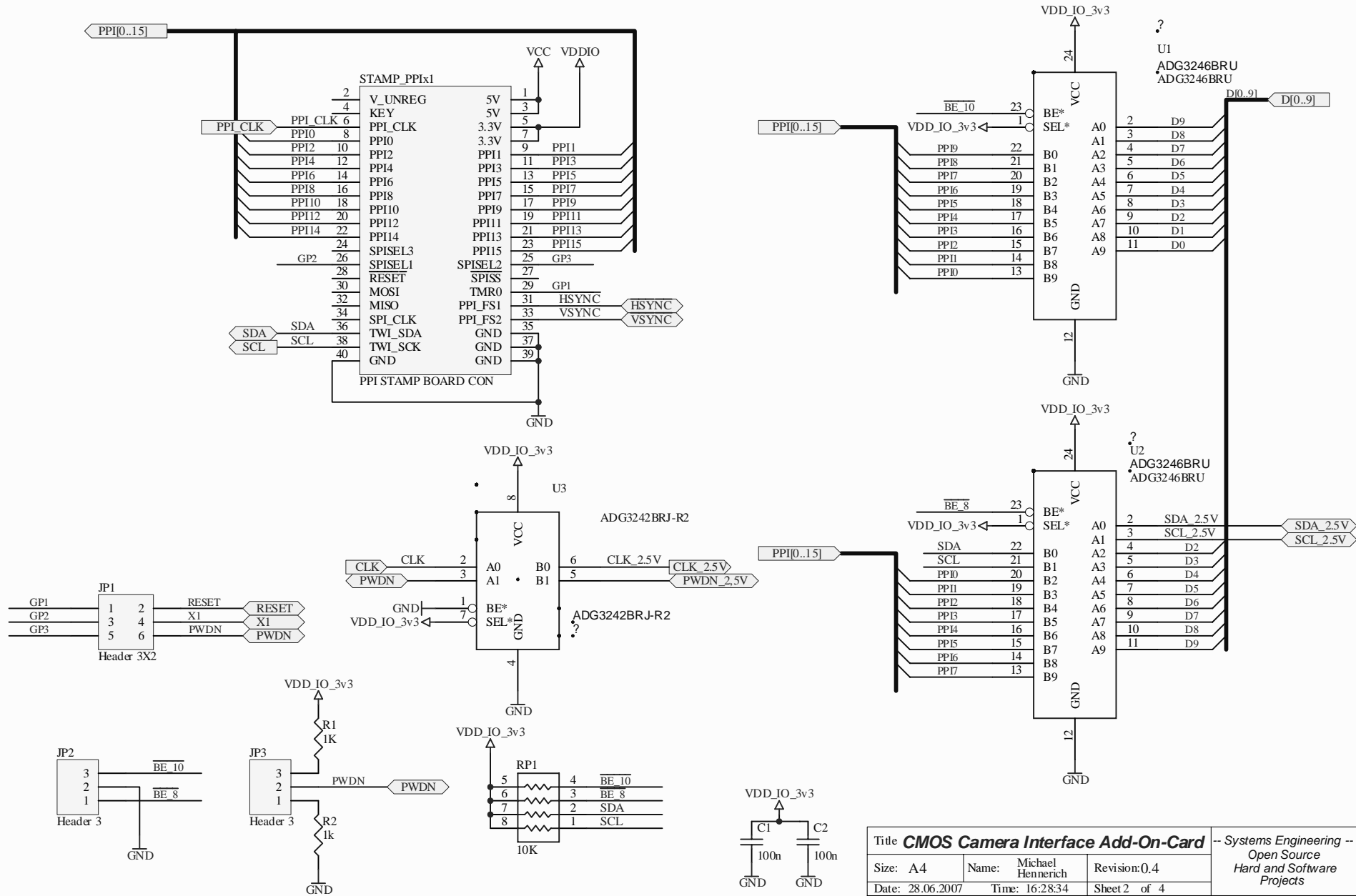


LOGO1

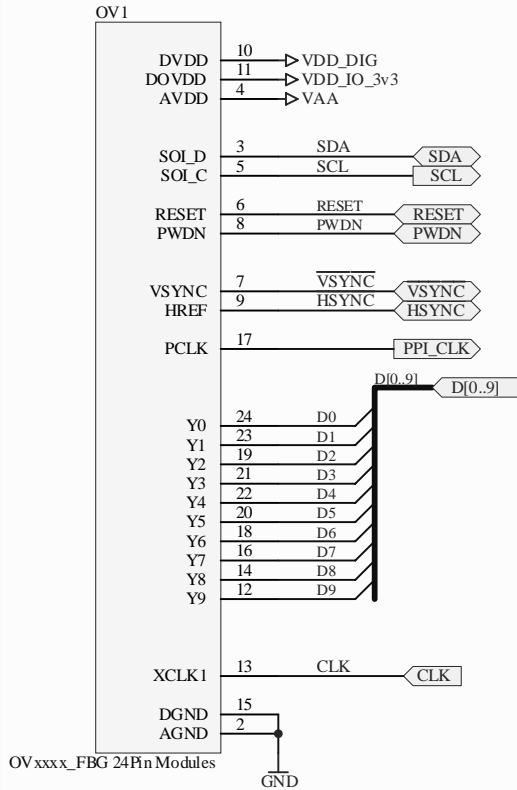


Title CMOS Camera Interface Add-On-Card			-- Systems Engineering -- Open Source Hard and Software Projects	
Size: A4	Name: Michael Hennerich	Revision:0.4		
Date: 28.06.2007	Time: 16:28:34	Sheet 1 of 4		
File: Toplevel CMOS Camera Interface.SchDoc				

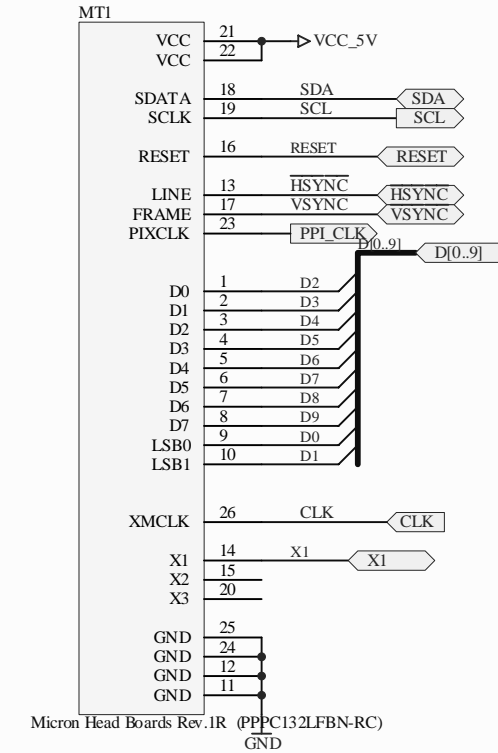
In 8-bit mode JP2 Set 1-2 D[2..9] are connected to PPI_D[0..7]
 In 10-bit mode JP2 Set 2-3 D[0..9] are connected to PPI_D[0..9]



In 8-bit mode JP2 Set 1-2 D[2..9] are connected to PPI_D[0..7]
 In 10-bit mode JP2 Set 2-3 D[0..9] are connected to PPI_D[0..9]



OVxxxx_FBG 24Pin Modules

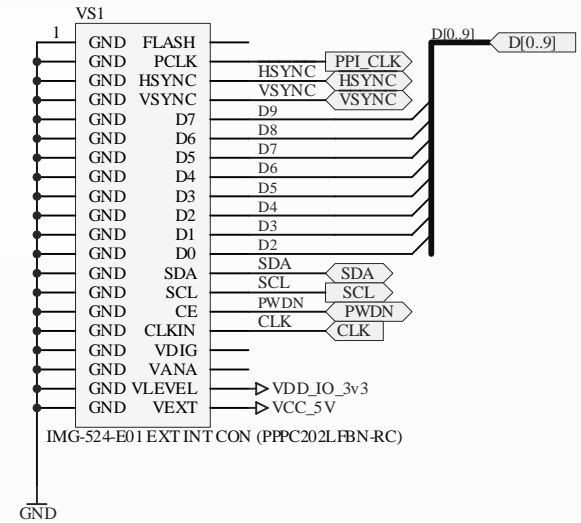


Micron Head Boards Rev.1R (PPPC132LFBN-RC)
 GND

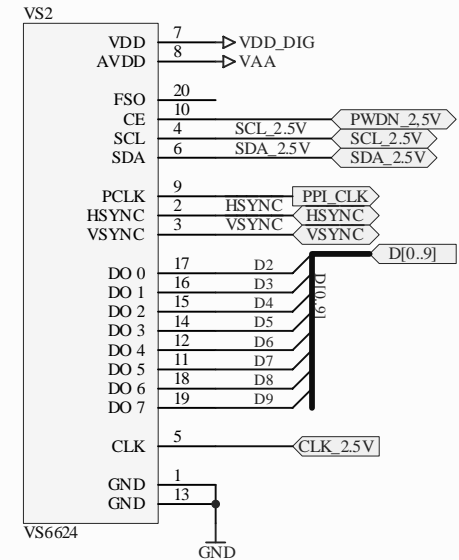
Micron MT9V022 REV:1R Camera Lens Board:
 Set SW1 to CLK27

ST X24 Evaluation Board:

- JP1 EXT_POWER (5V Supply form Blackfin Board)
- JP2 INT_VDIG (Use X24 on board voltage regulator)
- JP3 INT_VANA (Use X24 on board voltage regulator)
- JP4 INT_CLK (Use X24 on board crystal oscillator)
- JP5 EXT_CE (Blackfin controlled CE)
- JP6 EXT_SDA (Blackfin controlled SDA)
- JP7 EXT_SCL (Blackfin controlled SCL)



IMG-524-E01 EXT INT CON (PPPC202LFBN-RC)



VS6624

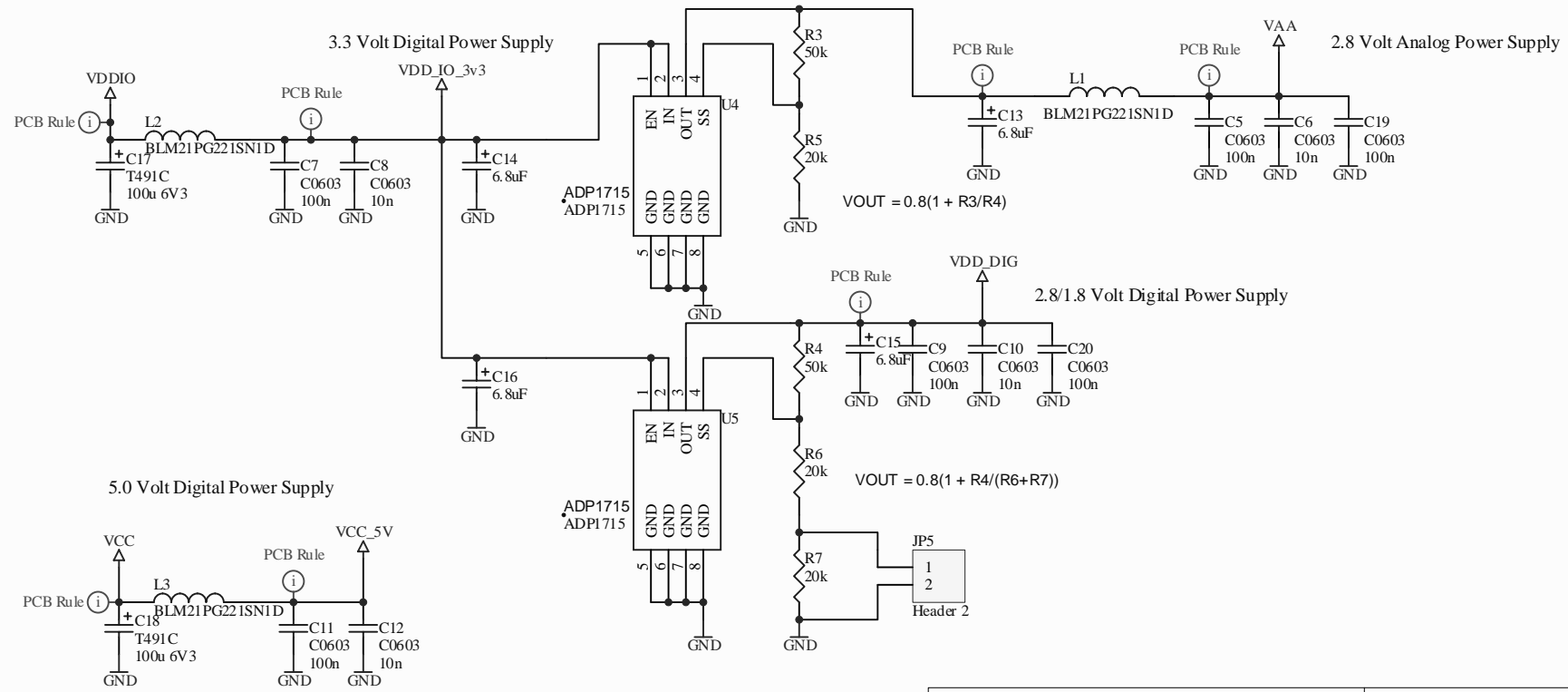
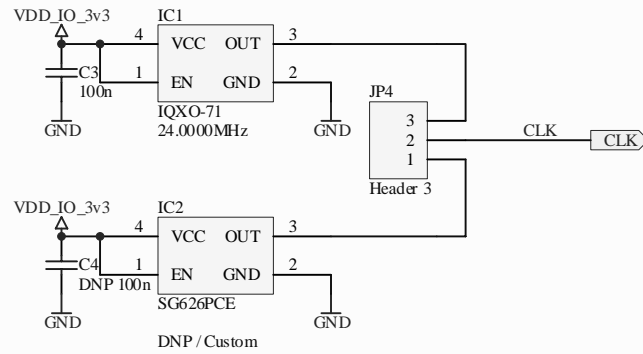
VS6624P0LP SMOP2 VGA 8x8, flex

Title CMOS Camera Interface Add-On-Card -- Systems Engineering --			
Size: A4	Name: Michael Hennerich	Revision:0.4	
Date: 28.06.2007	Time: 16:28:34	Sheet 3 of 4	
File: CAM Interface.SchDoc			

-- Systems Engineering --
 Open Source
 Hard and Software
 Projects



Clock Source



Title CMOS Camera Interface Add-On-Card			-- Systems Engineering -- Open Source Hard and Software Projects	
Size: A4	Name: Michael Hennerich	Revision: 0.4		
Date: 28.06.2007	Time: 16:28:34	Sheet 4 of 4		
File: Supply Clock.SchDoc				